



'সমানো মন্ত্র: সমিতি: সমানী'

UNIVERSITY OF NORTH BENGAL
B.Sc. Honours 3rd Semester Examination, 2023

CC7-PHYSICS

DIGITAL SYSTEMS AND APPLICATIONS

Time Allotted: 2 Hours

Full Marks: 40

The figures in the margin indicate full marks.

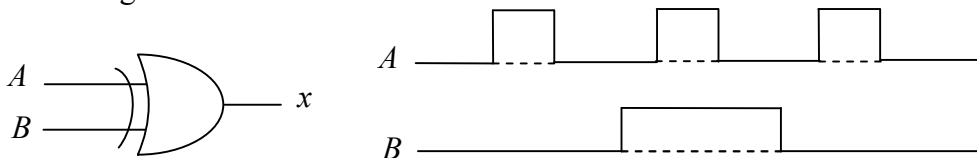
GROUP-A

1. Answer any **five** questions from following: 1×5 = 5
- (a) Choose the correct answer:
For a logical circuit there are n binary inputs. Then the number of different input combinations in the truth table is
- (i) $2n$ (ii) $2/n$ (iii) 2^n (iv) $2(n+1)$
- (b) In an Even parity scheme, which of the following words contain an error? Explain.
(i) 10110111 (ii) 11101010
- (c) Convert $(10011010101)_2$ to Octal.
- (d) Subtract $(1010)_2$ from $(1111)_2$ using 2's complement scheme.
- (e) Using Boolean algebra, verify $\bar{A}B(\bar{D} + \bar{C}D) + B(A + \bar{A}CD) = B$.
- (f) Write down full form of ASCII.
- (g) What is the decimal number represented by the BCD code 1010001111?
- (h) What is the minimum number of flip-flops required for a synchronous decade counter?

GROUP-B

Answer any three questions from the following 5×3 = 15

2. Draw the logic symbol of 4:1 DEMUX using basic gates. Write one application of multiplexer. 4+1
3. (a) Determine the output waveform x for the input waveforms A and B given below for a XOR gate. 2+3



- (b) Construct a Full Adder circuit using two Half adders and an OR gate and describe the operation.
4. (a) Derive the Boolean expression for a two input XOR gate to realize with two input NAND gates without using complemented variables and draw the circuit. 3+2
- (b) Simplify the Boolean expression $(A + B)(\bar{A} + C)(\bar{B} + D)(\bar{C}\bar{D})$.

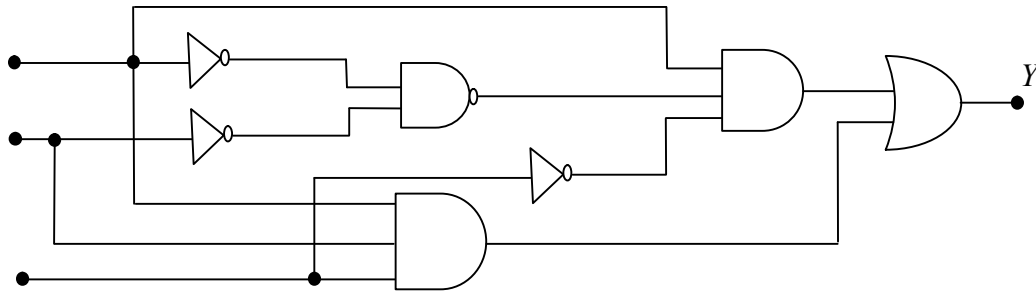
5. (a) Simplify the following expression using *K* map 3+2
 $f(A, B, C) = \sum m(2, 3, 4, 5) + \sum d(6, 7)$
- (b) What do you mean by Minterm and Maxterm?
6. What is a parity checker? Discuss how XOR gate can be employed as parity checker. 1+4

GROUP-C

Answer any *two* questions from the following

10×2 = 20

7. (a) Simplify the logic circuit given below and then implement the simplified circuit with logic gates. 4+4+2



- (b) With the help of logic diagram and truth table, explain a 3-line to 8-line decoder.
- (c) Distinguish between an encoder and a decoder.
8. (a) What advantage does a J-K flip-flop have over S-R flip-flop? 2+5+(1+2)
- (b) Construct the logic diagram of a master-slave JK flip-flop and explain the working principle.
- (c) What is D flip-flop? Show how an S-R flip-flop can be converted into a D flip-flop.
9. (a) Explain the operation of 4-bit serial in parallel out shift register. Give some applications of shift register. (4+2)+4
- (b) Construct Karnaugh map to design a logic circuit with minimum number of logic gates and implement the following truth table with logic circuit:

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

- 10.(a) Write short notes on any *two* of the following: 2+(1+4)+(1+2)
- (i) DRAM
- (ii) ALU
- (iii) CPU
- (iv) Mapping techniques.
- (b) Distinguish between synchronous and asynchronous counters. Describe with necessary diagrams the working of asynchronous counter.
- (c) What is multivibrator? Draw the circuit diagram of an astable multivibrator and explain its principle of operation.

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